Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OSC OUT**
2. **N/C**
3. **N/C**
4. **N/C**
5. **N. OEL**
6. **OEH**
7. **OSC LO1**
8. **GND**
9. **OUT**
10. **VCC**
11. **TRF**
12. **DIV A**
13. **OSC DR**
14. **DIVB**
15. **OSC LO2**
16. **DIV BB**
17. **OSC IN**
18. **N/C**

**.100”**

**MASK**

**REF**

**2 1 18 17 16 15**

**3**

**4**

**5**

**6**

**7 8 9 10**

**14**

**13**

**12**

**11**

**33C01**

**.100”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: 33C01**

**APPROVED BY: DK DIE SIZE .061” X .061” DATE: 2/7/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54ACT3301**

**DG 10.1.2**

#### Rev B, 7/1